# METHOD OF SELECTIVELY BUILDING RE-DUNDANT LOGIC STRUCTURES TO IM-PROVE FAULT TOLERANCE

## Abstract

A new hardware description language (HDL) extension at the register-transfer level (RTL) for designating particular logic functions as fault tolerant and a method of implementing a fault redundant scheme for the fault tolerant logic functions. Code (20) is written in VHDL at the RTL and includes instructions for adding the operator "FT" to certain logic functions. Logic functions that include the FT operator are considered critical functions, i.e., fault tolerant. By including the FT operator, a logic synthesis tool is alerted to the functions that have been designated as fault tolerant. As a result, the preprogrammed logic synthesis tool causes the design of the IC to include a fault redundant scheme (30) for the logic functions that include the FT operator. Fault redundant scheme (30) includes three copies of the logic function, i.e., Copy A (32), Copy B (34), and Copy C (36), as well as a majority voter 38.